

# Panel-Level Packaging RDL Production Solutions

Key technology to achieve semiconductor high-density packaging

# Manz AG — Cross-Domain Innovation Boost Industrial Upgrading

Manz develops and builds innovative and efficient production solutions to create industrial standards in the emerging sectors and industries. Our claim "engineering tomorrow's production" underscores our aspiration as an innovation driver for future markets.

With our innovative production solutions and extensive industrial experiences, we serve different sectors and industries. Our diversified positioning creates synergy effects from which our customers benefit greatly and ensure industrial development.

## Our equipment enables manufacturing process optimization and productivity improvement

Extensive expertise provides customers with dedicated solutions and services, which make a significant contribution to their success through faster, easier and more economical ways to achieve mass production goals and enable a faster time-to-market strategy.

## Introducing advanced interconnect structures to enable new packaging techniques

Manz specializes in advanced interconnect applications by providing portfolio includes both stand-alone tools and fully integrated solutions for the production of circuit patterns on substrates and other electronic interconnect systems. In addition, meet a wide range of customer requirements in lithographic and electroplating process tools. The further combination of Total Fab Services is joining software systems to make a cohesive infrastructure, enabling to work efficiently of the entire workflow.

A key factor to increase the system performance of the components is interconnect structures. The more densely chips packaging will require the more interconnect layers to integrate them all. Manz's solutions are designed for high-density redistribution layers (RDL) in the panel-level packaging process. This gives customers a significant competitive advantage to fulfill demands for future electronic devices.



#### Manz AG

- Established in 1987
- Headquarters in Reutlingen, Germany
- Other branches in Slovakia, Hungary, Italy, China, Taiwan, the US
- Approx. 1,400 employees worldwide, including around 500 engineers

#### Core technologies

- Assembly
- Inspection Systems
- Digital Printing

## Ever-Evolving Advanced Packaging Technologies to Drive Innovation

Moving to high portability and multi-functionality for electronics, also with AloT, 5G, and smart vehicles, the ICs are required compact, better performance & cost-effective. This led to a boom in advanced packaging technologies.

Nowadays, advanced packaging technologies are widely applying the attractive solutions of multi-die heterogeneous integration. The emerging applications such as high-performance computing, smart appliances and sophisticated electronic devices drive the growth of Fan-Out packaging solutions. The system structure and performance ratings of silicon chips will be varied by these massive changes. The overall features include,

- Smaller chips and smaller packaging size
- The increasing I/O counts to integrate multi-die and increase device efficacy
- Improved electronic circuitry performance and heat dissipation

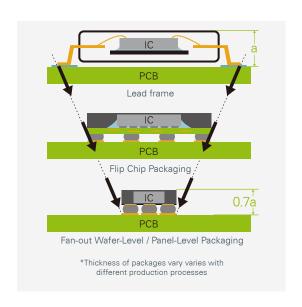
The current development of advanced packaging technologies is expecting further cost reduction by scaling up the production capacity. There are significant advantages to be derived from shifting from round silicon wafers to larger and rectangle-sized substrates like panels or PCBs. These technologies enable the continued increase in manufacturing areas and ramp up the production throughput.

### Fan-Out Panel Level Packaging technologies boost productivity & reduce costs

Meanwhile, the emerging AloT, 5G and smart vehicle applications also raise the high demand of semiconductor chips. Taking the sensor ICs as an example, although the line width and spacing (L/S) process requirements are decreasing, the trend is going to focus on the manufacturing cost reduction by leveraging the integrated packaging technologies of multi-die.

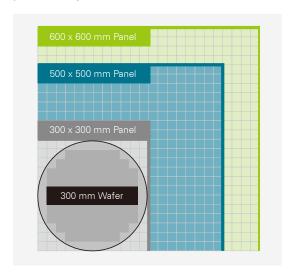
One of the key benefits of Fan-Out packaging is reducing PCB size because of ultra-compact ICs. This enables a small form factor electronic design to make the electronics products using fewer components, smaller PCBs, compact physical dimensions, in short, a better cost structure implementation. This approach also provides the extra space for accommodating other new electronic components.

The manufacturing area of FOWLP is less than 85 % of a wafer. But FOPLP can have better usage to use around 95 % and above. The produced IC chip counts in one glass substrate are higher. As chip yield rates improved, these advantages will reach 5.7 times compared with one 300 mm wafer.



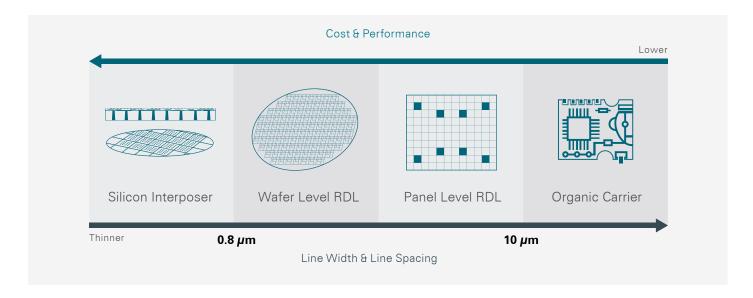
## Advanced packaging technologies evolve rapidly

Applying FOPLP, a thinner package can be achieved effectively with the essential benefits of increasing performance, more rooms for more components, less production cycles and thus cost reduction.



# Competitive Advanced Fan-Out Packaging Shapes the Future of Chip Designs

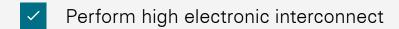
The Fan-out packaging technologies vary by a multitude of process solutions. It leads the severe competition in different market segments. Especially in FOWLP and FOPLP processes, there are key distinctions in terms of cost and performance.



# FOWLP and FOPLP techniques have both been winners in different ways

FOWLP and FOPLP technologies were designed for integrating multiple ICs as a single package through heterogeneous integration. And at the same time, it also embedded power and passive components applying RDL interconnects to form a smaller electronics system.

Critical challenges:



- Provide high uniformity
- High resolution RDL

FOWLP / FOPLP Characteristics:

#### **FOWLP**

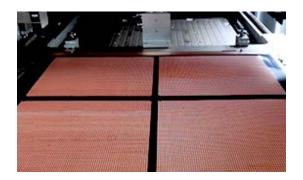
- Suitable for high-density fan-out packaging
- Require high precision manufacturing and advanced equipment
- Thinner line width
- Limited IO counts from 300 to 1500
- Suitable for manufacturing of APE, CPU, GPU and FPGA chips

#### **FOPLP**

- Focus on high-power, high-current semiconductor devices and applications
- Less requirements for process equipment
- Less requirements of fine pitch and line width & spacing
- The IO counts limitation from 10 to 500 only
- Suitable for manufacturing of APE, power ICs and power management ICs chips

# High-Tech Industries Gear up for FOPLP Development and Provide Upbeat Outlook

The revolution of advanced packaging technology is driven by different manufacturers through either process technologies or production lines revival. Aim to provide cost & performance effective components that enabling 5G, AloT and other smart solutions.





Advanced packaging attracts players with many different business models, including IDM, OSAT, foundry, PCB, IC substrate and panel makers. The competition between them is enabling integrated trends to achieve multi-chip integration with powerful performance in the future.

As a globally recognized and trusted manufacturer, Manz provides integrated solutions with diverse technological expertise for manufacturers who are keen to be a player in panel-level packaging

### OSAT, IDM and foundry services

Looking at front-end process IDM or foundry service providers, the downstream integration with chip packaging, it is an attractive and profitable service model. In the back-end services, the OSAT vendors can get benefits from their existing production experience by quickly incorporating FOPLP technology. The semiconductor supply chains can gain a competitive edge to find cost advantage and product competitiveness.

#### PCB and IC substrate manufacturers

Simultaneous design flow of a single chip, package, and PCB is becoming more important. The PCB vendors can fast enter the advanced packaging market by adapting FOPLP technologies to gain process know-how through the upgrade or improve equipment. Originally, the indispensable suppliers of PCB and IC substrate have suffered declining market penetration rates. The needs to adjust the development directions by increasing the Front-end process tools are able to catch up the rapid trends and maintain the leading position.

## Display panel makers

The processing area of a 300 mm wafer is about 15 % of a Generation 3.5 (620 imes 750 mm) glass substrate. The glass substrate has scaling advantages. The old Generation 3.5 panel production lines can be transformed into the FOPLP process to produce higher-value RDL-based chips by upgrading equipment and migrating processes. FOPLP technology not only supplies end products with higher efficacy, it also provides higher cost-efficiency.

# Cross-Domain Innovation Leading FOPLP to Success — Cu RDL Technology

Through the fined copper interconnection of RDL technology, the single silicon is either to connect different functions of the chip to the passive components in 2D, or through 3D structures. Both techniques integrate multiple chips with excellent cost & performance.

The copper interconnection of RDL technology is critical for FOPLP



### Decreasing package thickness

To draw the trace of needed RDL from the multiple dies does not require a substrate, nor a wire-bond. This will further reduce the package thickness when multiple chips are stacked



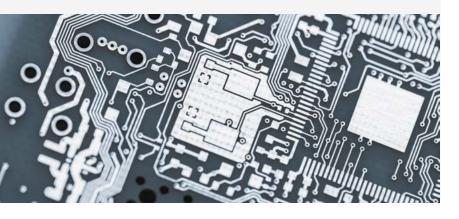
## Simplifying process flow and reducing material costs

Multi-die interconnection through RDL process in fan-out packaging for stacking multiple chips simultaneously, this will increase more than ten times of performance and reduce packaging thickness. Furthermore, it will benefit to drive process simplification and cost reduction.



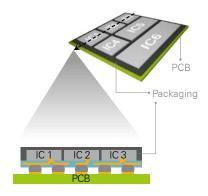
## Strengthening the foundation of homogeneous or heterogeneous integration

The single multi-functional integrated chip through RDL interconnect could fabricate either the same silicon dies or different ICs to a glass substrate or other semiconductor material. This method will integrate full systems into one single packaging chip and massively simplify the digital design flow.



### Advanced interconnection by RDL is an integral part of the **FOPLP**

The rising demand of modern electronics is boosting the technology of homogeneous or heterogeneous integration. Leveraging the RDL process, the latest multi-chip packaging trends are shifting from PCB or IC substrate to advanced integration technologies such as thin film process or 2.5D silicon interposer.



#### Further information

Fan-out package technique creates more I/O contacts on the package, hence to reduces the packaging dimension to accomplish the heterogeneous integration.

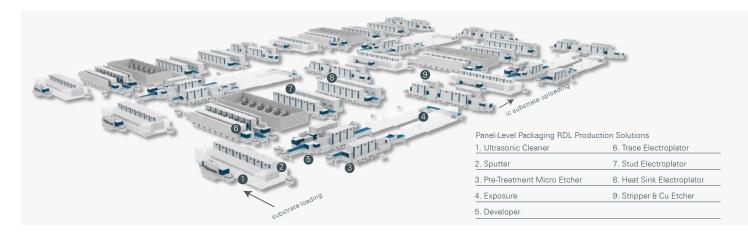
The process includes:

- 1) dicing a wafer.
- 2) mounting known good dies (KGD) on a carrier for molding.
- 3) RDL and solder bump formation.
- 4) separate molding and reusable carrier.

# Manz's Multiple Core Technologies with Diverse

# Manufacturing Expertise

Manz developed lithography tools and electroplating systems for achieving a high density of RDL process. More, by integrating Manz automation, Manz is dedicated to helping customers optimize processes with high quality, high productivity and low manufacturing cost.



Extensive experience in automation, wet chemistry, electroplating equipment and rich process know-how of RDL technology. This enables Manz to offer customized and high-efficiency integrated manufacturing solutions to fulfill the requirements of FOPLP technology.

# Manz FOPLP RDL production solutions with proven records for mass production

#### Automation

AGV | EFEM | Loading & Unloading System
 | Robotics | Spectrum Analyzer

### Wet chemistry

Cleaner | Developer | Etcher | Stripper

## Electroplating

Jig-free Vertical Electroplating

The best practices to optimize production

# Full services from equipment to production fab planning

- High-precision product equipment manufacturing
- Fully automatic production system
- Big data analytics in manufacturing process
- Simulation & fab planning/implementation

# Suitable for various substrate for production

■ FR4 | PI | Stainless steel | Glass

# Key numbers of production optimization

- Electroplating uniformity >90 %
- High precision inline chemistry analyzer reaching 97 % of stability
- L/S range:  $10\mu m / 10\mu m$  to  $20\mu m / 20\mu m$

## **Our Locations**

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